IN THE UNITED STATES DISTRICT COURT

FOR THE DISTRICT OF DELAWARE

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| INTELLECTUAL VENTURES I LLC and INTELLECTUAL VENTURES II LLC, | ) | |
| Plaintiffs/Counterclaim Defendants, | ) | |
| v. | ) | Civ. No. 13-453-SLR |
| TOSHIBA CORPORATION, TOSHIBA AMERICA, INC., TOSHIBA AMERICA ELECTRONIC COMPONENTS, INC., and TOSHIBA AMERICA INFORMATION SYSTEMS, INC., | ) | |
| Defendants/Counterclaim Plaintiffs. | ) | |

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**MEMORANDUM OPINION**

Dated: December 19, 2016
Wilmington, Delaware

**ROBINSON, District Judge**

## I. INTRODUCTION

Plaintiffs Intellectual Ventures I LLC and Intellectual Ventures II LLC ("IV") filed suit against Toshiba America Electronic Components, Inc., Toshiba America, Inc., Toshiba America Information Systems, Inc., and Toshiba Corporation ("Toshiba") on March 20, 2013 alleging that various Toshiba products (collectively, "the accused products") infringe ten patents (collectively, "the patents"). (D.I. 1) The court issued a claim construction order on December 17, 2015. (D.I. 277) Through the course of this litigation, IV has voluntarily dismissed, agreed to stay or stipulated to summary judgment of noninfringement of five of the asserted patents. (D.I. 171, 175, 323, 360, and 392) U.S. Patent Nos. 6,618,788 ('788 patent), 5,938,742 ('742 patent), 5,568,431 ('431 patent), 5,500,819 ('819 patent), and 5,701,270 ('270 patent) remain at issue. Trial is scheduled to commence on January 17, 2017.

On July 21, 2016, Toshiba filed a motion for partial summary judgment for claim priority of the '270 patent and invalidity of claims 10 and 24 of the '788 patent. (D.I. 420) Toshiba also filed a motion for summary judgment of noninfringement of the patents. (D.I. 427) IV moved for summary judgment of no available noninfringing alternatives with respect to the patents; no invalidity with respect to six prior art references in a "practicing the prior art" defense; no invalidity with respect to six prior art references dependent on a claim construction question; no invalidity with respect to the patents; and reference estoppel from an *inter partes* review of the '819 patent. (D.I. 426) On August 15, 2016, Toshiba filed a motion to exclude opinions and testimony from IV's damages expert, David J. Teece ("Teece"). (D.I. 449) Toshiba also moved to strike portions of a supplemental expert report from one of IV's experts, Joseph McAlexander ("McAlexander"). (D.I. 453) IV moved to exclude testimony from Toshiba's damages expert, Julie L. Davis ("Davis"). (D.I. 457) IV also filed a motion for

relief based upon allegations that Toshiba made untimely infringement and validity theories. (D.I. 460) These motions are presently before the court. The court has jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

## II. BACKGROUND

### A. The Parties

IV is a limited liability company organized and existing under the laws of the State of Delaware, with a principal place of business in Bellevue, Washington. (D.I. 1 at ¶ 1) Toshiba Corporation is a Japanese corporation with a principal place of business in Tokyo, Japan. Toshiba America, Inc. ("TAI") is a Delaware corporation with a principal place of business in New York City, New York. Toshiba America Electronic Components, Inc. ("TAEC") is a California corporation with its principal place of business in Irvine, California. Toshiba America Information Systems, Inc. ("TAIS") is a California corporation with a principal place of business in Irvine, California. (D.I. 35 at 1-2)

### B. The Patents

There remain five patents at bar: the '788 patent, entitled "ATA device control via a packet-based interface," was filed on September 27, 2000 and issued on September 9, 2003; the '742 patent, entitled "Method for configuring an intelligent low power serial bus," was filed on August 18, 1995 and issued on August 17, 1999; the '431 patent, entitled "Memory architecture and devices, systems and methods utilizing the same," was filed on September 21, 1995 and issued on October 22, 1996; the '819 patent, entitled "Circuits, systems and methods for improving page accesses and block transfers in a memory system," was filed on September 30, 1994 and issued on March 19, 1996; and the '270 patent, entitled "Single chip controller-memory device with interbank cell replacement capability and a memory architecture and methods suit[a]ble

for implementing the same," was filed on February 1, 1996 and issued on December 23, 1997.

## III. STANDARD OF REVIEW

"The court shall grant summary judgment if the movant shows that there is no genuine dispute as to any material fact and the movant is entitled to judgment as a matter of law." Fed. R. Civ. P. 56(a). The moving party bears the burden of demonstrating the absence of a genuine issue of material fact. *Matsushita Elec. Indus. Co. v. Zenith Radio Corp.*, 415 U.S. 475, 586 n. 10 (1986). A party asserting that a fact cannot be—or, alternatively, is—genuinely disputed must be supported either by citing to "particular parts of materials in the record, including depositions, documents, electronically stored information, affidavits or declarations, stipulations (including those made for the purposes of the motions only), admissions, interrogatory answers, or other materials," or by "showing that the materials cited do not establish the absence or presence of a genuine dispute, or that an adverse party cannot produce admissible evidence to support the fact." Fed. R. Civ. P. 56(c)(1)(A) & (B). If the moving party has carried its burden, the nonmovant must then "come forward with specific facts showing that there is a genuine issue for trial." *Matsushita*, 415 U.S. at 587 (internal quotation marks omitted). The court will "draw all reasonable inferences in favor of the nonmoving party, and it may not make credibility determinations or weigh the evidence." *Reeves v. Sanderson Plumbing Prods., Inc.,* 530 U.S. 133, 150 (2000).

To defeat a motion for summary judgment, the non-moving party must "do more than simply show that there is some metaphysical doubt as to the material facts." *Matsushita*, 475 U.S. at 586-87; *see also Podohnik v. U.S. Postal Service*, 409 F.3d 584, 594 (3d Cir. 2005) (stating party opposing summary judgment "must present more than just bare assertions, conclusory allegations or suspicions to show the existence of a genuine issue") (internal quotation marks omitted). Although the "mere existence of

some alleged factual dispute between the parties will not defeat an otherwise properly supported motion for summary judgment," a factual dispute is genuine where "the evidence is such that a reasonable jury could return a verdict for the nonmoving party." *Anderson v. Liberty Lobby, Inc.*, 477 U.S. 242, 247-48 (1986). "If the evidence is merely colorable, or is not significantly probative, summary judgment may be granted." *Id.* at 249-50 (internal citations omitted); *see also Celotex Corp. v. Catrett*, 477 U.S. 317, 322 (1986) (stating entry of summary judgment is mandated "against a party who fails to make a showing sufficient to establish the existence of an element essential to that party's case, and on which that party will bear the burden of proof at trial").

## IV. DISCUSSION

### A. '788 Patent

#### 1. Claim construction

The parties disagree over the construction of two terms found in claims 10 and 24 of the '788 patent. These terms are "ATA device" and "a given ATA register-delivered transaction."

##### a. Standard

Claim construction is a matter of law. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1330 (Fed. Cir. 2005) (en banc). Claim construction focuses on intrinsic evidence - the claims, specification, and prosecution history - because intrinsic evidence is "the most significant source of the legally operative meaning of disputed claim language." *Vitronics Corp. v. Conceptronic, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996); *Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 979 (Fed. Cir. 1995) (en banc), *aff'd*, 517 U.S. 370 (1996). Claims must be interpreted from the perspective of one of ordinary skill in the relevant art at the time of the invention. *Phillips*, 415 F.3d at 1313. In some cases, "the district court will need to look beyond the patent's intrinsic evidence and to consult

extrinsic evidence in order to understand, for example, the background science or the meaning of a term in the relevant art during the relevant time period." *Teva Pharm. USA, Inc. v. Sandoz, Inc.*, _ U.S. _, 135 S. Ct. 831, 841 (2015) (citation omitted).

Claim construction starts with the claims and remains centered on the words of the claims throughout. *Interactive Gift Express, Inc. v. Compuserve Inc.*, 256 F.3d 1323, 1331 (Fed. Cir. 2001). In the absence of an express intent to impart different meaning to claim limitations, "the words of a claim are generally given their ordinary and customary meaning," which is "the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention." *Phillips*, 415 F.3d at 1312-13 (quoting *Vitronics*, 90 F.3d at 1582). "The ordinary meaning may be determined by reviewing various sources, such as the claims themselves, the specification, the prosecution history, dictionaries, and any other relevant evidence. Ultimately, '[t]he only meaning that matters in claim construction is the meaning in the context of the patent.'" *Ruckus Wireless, Inc. v. Innovative Wireless Sols., LLC*, Civ. No. 2015-1425, _ F.3d. _, 2016 WL 3065024, at *3 (Fed. Cir. May 31, 2016). The specification is often "the single best guide to the meaning of a disputed term." *Phillips*, 415 F.3d at 1315.

**b. Analysis**

**i. "ATA device"**

During claim construction, the parties agreed that an "ATA device" is "a data device that complies with an ANSI (American National Standards Institute) ATA standard." (D.I. 183 at 5) The parties now disagree whether, for purposes of the '788 patent, this term includes devices compliant with ATA specifications introduced after the filing of the application that led to the '788 patent. (*See, e.g.*, D.I. 494 at 28-30) Toshiba's expert, Thomas E. Gardner ("Gardner"), in his expert report "use[s] the term 'ATA Standard' to apply generically to the four standards existing prior to the filing date

of the '788 patent, and any specific citation herein will be to the ATA-4 Standard."[1] (D.I. 423 at ¶ 42) IV's expert, Robert Dezmelyk ("Dezmelyk"), opines that the "ATA device" and "ATA interface" terms in the '788 patent should include the ATA/APAPI-5, ATA/ATAPI-6, and ATA/ATAPI-7 standards introduced in 2000, 2002, and 2005. (D.I. 442, ex. 3 at 11-12) Dezmelyk also identified the ATA8-ACS specification from 2007 as critical to the linkage between the SATA specification and the ATA specification. (*Id.* at 13) IV contends that the '788 patent supports such an interpretation, because it contemplates future ATA standards. ('788 patent, 1:15-17; *see also* D.I. 494 at 28)

The agreed upon construction for "ATA device" is "a data device that complies with an . . . ATA standard," which mirrors language in the specification. (D.I. 183 at 5; '788 patent, 1:11-13) The specification does not limit the term to specific versions of the ATA standard, and states that "[f]uture ATA standards are currently contemplated." (*Id.*, 1:15-17) Moreover, the agreed definition requires compliance with "an" ATA standard. The "ATA" acronym appears in this phrase as an adjective modifying "standard." "An" is an indefinite article, used as an alternative to "a" "in speech and writing before words beginning with a vowel sound." *Merriam-Webster Unabridged* (2016). "A" is "used before most singular nouns other than proper and mass nouns when the individual in question is undetermined, unidentified, or unspecified." *Id.* Read together "an . . . ATA standard" suggests that the ATA standard is not specified; therefore, the court construes "ATA device" as "a data device that complies with an ANSI (American National Standards Institute) ATA standard, where the specific ATA standard is not identified, and any ATA standard will suffice."

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[1] "The number of ATA and/or ATAPI commands described in ATA standards has increased over time from 33 in ATA-114 to 77 in ATA-8." (D.I. 422, ex. 2 at ¶22 (Gardner supplemental expert report on invalidity))

### ii. "Given ATA register-delivered transaction"

Claims 10 and 24 of the '788 patent each recite "receiving a packet comprising an ATA command block from a remote host, the ATA command block comprising the ATA register accesses necessary to execute a given ATA register-delivered transaction." ('788 patent, 14:35-38; 16:17-20) The ATA command block includes the information (the ATA register accesses) necessary to "execute a given ATA register-delivered transaction," but the specification does not define the term. ('788 patent, 4:13-21, 13:3) IV argues that "a person of ordinary skill in the art would understand that the "given ATA register limitation requires the capability to execute any ATA register-delivered transaction (i.e., the full set of ATA register delivered transactions), and not merely the capability to execute only one ATA register-delivered transaction." (D.I. 440 at 58-59) (emphasis omitted) Toshiba argues that the "'given ATA register-delivered transaction' [term] may be satisfied by at least one given ATA register-delivered transaction." (D.I. 486 at 33)

A "benefit" of the embodiments disclosed in the '788 patent is to use "a USB plug-and-play connection to access an external . . . hard drive or other . . . device." ('788 patent, 3:54-57) "This allows the main benefits of an ATA hard drive (large storage size at low cost) to be offered in a portable or add-on configuration." (*Id.*, 3:57-59) The specification states that "these embodiments can allow a host to have full flexible access to an ATAPI device's ATA registers and to execute up to the full set of ATA commands that the ATAPI device can recognize." (*Id.*, 3:59-62) At the same time, the specification includes a statement that "[a]n ATAPI device supports a very small subset of the traditional ATA command set." (*Id.*, 2:36-38; *see also* D.I. 440 at 58-58) The specification discloses prior art, in the form of "ATAPI-over-USB functionality," and discusses some of its limitations:

> For instance, there is no mechanism to allow full visibility by ATAPI driver into the registers of ATAPI device 100—when ATAPI driver 82 issues an

> ATAPI command, it receives back only a status indication as to whether the command passed, failed, or caused a phase error. Perhaps even more important, the configuration in FIG. 3 only allows the host to issue ATAPI packet-delivered commands to ATAPI devices.

('788 patent, 3:44-51)

The specification discloses that a host may go beyond ATAPI and access "external ATA hard drive[s] or other non-ATAPI ATA device[s]." ('788 patent, 3:56-57) Read together, the specification teaches that (1) an ATAPI device "supports a very small subset of the traditional ATA command set," (2) known approaches such as ATAPI-over-USB do not "allow full visibility . . . into the registers of the ATAPI device," and (3) the disclosed embodiments "can allow a host to have full flexible access to an ATAPI device's ATA registers and to execute up to the full set of ATA commands the ATAPI device can recognize." ('788 patent, 2:36-38, 3:45-46, 3:59-62) Here, the "full set" refers to the commands "the ATAPI device can recognize," and not to the entire set of universally available ATA commands. This is the only part of the specification to employ this "full set" language, and no other part of the specification discusses "all," "any," or "the full set" of ATA commands.[2] Significantly, claims 10 and 24 are not limited to ATAPI devices,[3] and presumably encompass non-ATAPI ATA devices to which the above discussion does not apply.

The claims recite "a given . . . transaction" and "the given . . . transaction." ('788 patent, 14:37-38, 14:40-41, 14:45, 16:19-20, 16:22-23, 16:27) "A given" means "definitely stated," which is synonymous with the words "fixed" and "specified." *Merriam-Webster Unabridged* (2016). The word "transaction" appears in the singular,

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[2] Elsewhere, the specification discloses at least one scenario in which the host accesses less than the full set of ATA commands. For example, in the disclosed embodiment with reference to figure 11, the host specifically cannot initiate the ATA PACKET command. ('788 patent, 12:59-63)

[3] ATAPI only appears as a limitation in dependent claims 8 and 22, both of which depend on independent claims that are not asserted here.

and read together with "a given" suggests that the claim refers to a definitely stated transaction, which is also singular; therefore, a "given . . . transaction" is a single, definitely stated transaction. As a result, the court reads the "a given ATA register-delivered transaction" and "the given ATA register-delivered transaction" limitations as being "satisfied by at least one given ATA register-delivered transaction." (D.I. 486 at 33)

**2. Noninfringement**

Toshiba moves for summary judgment of noninfringement of claims 10 and 24 of the '788 patent. (D.I. 427)

**a. Standard**

When an accused infringer moves for summary judgment of noninfringement, such relief may be granted only if one or more limitations of the claim in question do not read on an element of the accused product, either literally or under the doctrine of equivalents. *See Chimie v. PPG Indus., Inc.*, 402 F.3d 1371, 1376 (Fed. Cir. 2005); *see also TechSearch, L.L.C. v. Intel Corp.*, 286 F.3d 1360, 1369 (Fed. Cir. 2002) ("Summary judgment of noninfringement is . . . appropriate where the patent owner's proof is deficient in meeting an essential part of the legal standard for infringement, because such failure will render all other facts immaterial."). Thus, summary judgment of noninfringement can only be granted if, after viewing the facts in the light most favorable to the non-movant, there is no genuine issue as to whether the accused product is covered by the claims (as construed by the court). See *Pitney Bowes, Inc. v. Hewlett–Packard Co.*, 182 F.3d 1298, 1304 (Fed. Cir. 1999).

**b. Analysis**

IV argues that the accused products infringe claims 10 and 24 of the '788 patent because, for example, "every SATA-compliant implementation must contain the

disputed 'ATA device' and 'ATA interface'" found in claims 10 and 24. (D.I. 494 at 23) IV's expert, Dezmelyk, based his infringement opinion primarily on Toshiba's product literature, which stated that the products comply with the SATA specification,[4] and this fact is not disputed. (D.I. 442, ex. 1 at 97) In his opening expert report, Dezmelyk stated that a "system configured in accordance with the mandatory aspects of SATA Revision 1.0 and all subsequent versions, revisions, updates, and sub-versions of the SATA specifications . . . includes every limitation of claim 24 . . . . [and] performs every step of claim 10."[5] (*Id.*) Toshiba argues in response that IV has "failed to show that compliance with the SATA specifications necessarily results in infringement." (D.I. 530 at 15)

As noted, IV bases its infringement argument on compliance with the SATA standard. *See Fujitsu Ltd. v. Netgear Inc.*, 620 F.3d 1321, 1327 (Fed. Cir. 2010). There seems to be no dispute that, with respect to the '788 patent, the accused products practice the SATA standards; the experts apparently disagree about whether the relevant SATA standards satisfy the claim limitations, specifically because they relate to ATA devices and ATA interfaces. These are issues of fact that are best resolved by a jury. For these reasons, the court denies Toshiba's motion for summary judgment of noninfringement of the '788 patent.

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[4] According to Dezmelyk, "the evidence I'm using to rely on that is the documentation, standards and as I understand it representations in documents from Toshiba that say they do [comply with the SATA specification] and, of course, the fact that they actually do. If you take one of these things in the real world, they actually work." (D.I. 495, ex. E at 4)

[5] "Exhibit C" associated with Dezmelyk's April 8, 2016 report apparently explains how all devices that practice the SATA specification infringe claims 10 and 24 of the '788 patent. (D.I. 442, ex. 1 at 97, ex. 3 at 12, 13, and 14)

### 3. Invalidity

Toshiba moves for partial summary judgment of invalidity of claims 10 and 24 of the '788 patent as anticipated by the ANSI draft specification for IEEE 1394 to AT Attachment ("Tailgate")[6] reference. (D.I. 420; D.I. 421 at 8) The parties agree that Tailgate is prior art to the '788 patent. (*Id.*; D.I. 440 at 55-60) IV contends that Tailgate does not anticipate claims 10 or 24, "because it lacks an 'ATA command block comprising the ATA register addresses necessary to execute a given ATA register-delivered transaction,'" and this is the only claim limitation in dispute. (D.I. 440 at 60) IV argues that "the '788 patented invention is able to execute the full set of ATA commands,"[7] and Tailgate cannot execute the **full set** of ATA commands.[8] (D.I. 440 at 57) Toshiba agrees that, in Tailgate, "the ATA Command Block does not specify values for the Alternate Status and Device Control registers." (D.I. 421 at 17)

#### a. Standard

Under 35 U.S.C. § 102(b), "[a] person shall be entitled to a patent unless the invention was patented or described in a printed publication in this or a foreign country . . . more than one year prior to the date of the application for patent in the United States." The Federal Circuit has stated that "[t]o anticipate a claim, a single prior art reference must expressly or inherently disclose each claim limitation." *Finisar Corp. v. DirecTV Grp. Inc.*, 523 F.3d 1323, 1334-35 (Fed. Cir. 2008) (quoting *Celeritas Techs., Ltd. v. Rockwell Int'l Corp.*, 150 F.3d 1354, 1361 (Fed. Cir. 1998)). "Anticipation requires that the reference describe not only the elements of the claimed invention, but

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[6] (*See generally* D.I. 424, ex. 4)

[7] IV cited to table 2 of the specification to demonstrate these commands. ('788 patent, 8:25-35) The specification does not discuss table 2. IV's expert, Dezmelyk, explained that table 2 "discloses an example of registers [sic] accesses required to execute a given transaction." (D.I. 442, ex. 2 at 84)

[8] Tailgate recites that the "Alternate Status and Device Control registers are not addressable." (D.I. 424, ex. 4 at 40)

also that it describe those elements arranged as in the claim." *Enfish, LLC v. Microsoft Corp.*, _ F.3d _, Civ. No. 2015-1244, 2016 WL 2756255, at *11 (Fed. Cir. May 12, 2016) (internal quotations omitted).

"The explicit claim limitations must be considered in [the] determination of anticipation." *In re Schreiber*, 128 F.3d 1473, 1481 (Fed. Cir. 1997). In determining whether a patented invention is explicitly anticipated, "the proponent must show 'that the four corners of a single, prior art document describe every element of the claimed invention,'" "arranged or combined in the same way as in the claim." *Net MoneyIN, Inc. v. VeriSign, Inc.*, 545 F.3d 1359, 1370 (Fed. Cir. 2008). The claims are read in the context of the patent specification in which they arise and in which the invention is described. *Glaverbel Societe Anonyme v. Northlake Mktg. & Supply, Inc.*, 45 F.3d 1550, 1554 (Fed. Cir. 1995). The prior art need not be *ipsissimis verbis* (i.e., use identical words as those recited in the claims) to be anticipating. *Structural Rubber Prods. Co. v. Park Rubber Co.*, 749 F.2d 707, 716 (Fed. Cir. 1984).

An anticipation inquiry involves two steps. First, the court must construe the claims of the patent in suit as a matter of law. Second, the finder of fact must compare the construed claims against the prior art. *In re Montgomery*, 677 F.3d at 1379. Anticipation, an invalidity defense, must be proven by clear and convincing evidence. *Microsoft Corp. v. i4i Ltd.*, 564 U.S. 91, 95 (2011).

**b. Analysis**

IV asserts that "Tailgate [] does not anticipate claims 10 and 24 of the '788 patent because it does not disclose the capability to execute the full set of ATA commands, . . . and thus lacks . . . [the] 'given ATA register-delivered transaction' [limitation]." (D.I. 440 at 50) "To anticipate, every element and limitation of the claimed invention must be found in a single prior art reference, arranged as in the claim." *Brown v. 3M*, 265 F.3d 1349, 1351 (Fed. Cir. 2001) (citations omitted). "When a claim covers several

structures or compositions, . . . the claim is deemed anticipated if any of the structures or compositions within the scope of the claim is known in the prior art." *Id.*

In order for the Tailgate reference to anticipate claims 10 and 24 of the '788 patent, Tailgate must teach each limitation of the claims under a clear and convincing standard. For example, claim 10 recites:

> A method of operating a packet-to-ATA bridge, the method comprising:
>
> receiving a packet comprising an ATA command block from a remote host, the ATA command block comprising the ATA register accesses necessary to execute a given ATA register-delivered transaction;
>
> parsing the command block into a sequence of ATA register operations necessary to execute the given ATA register-delivered transaction;
>
> communicating with an ATA device attached to the bridge via an ATA interface to execute the sequence of ATA register operations on the ATA device; and
>
> when the given ATA register-delivered transaction requests the values for one or more registers on the ATA device, returning the register values to the host in packet format.

('788 patent, 14:33-48) The preamble of claim 24 recites "[a]n apparatus comprising a computer-readable medium containing computer instructions that, when executed, cause a processor or multiple communicating processors to perform a method for operating a packet-to-ATA bridging device." ('788 patent, 16:11-15) The apparatus of claim 24 performs the same method as is found in claim 10.

The preambles of claims 10 and 24 include the terms "packet-to-ATA bridge" and "packet-to-ATA bridging device," which the court construed to mean "[h]ardware or software that enables packet-to-ATA or ATA-to-packet transfer." (D.I. 277 at 18-19) Through its expert, Gardner, Toshiba has demonstrated that a "packet-to-ATA bridge" is disclosed in figure 3 of the Tailgate reference. (D.I. 424, ex. 4 at 26; D.I. 421 at 13-14; *see also* D.I. 422, ex. 4 at 2-4, 24-26) Toshiba has also demonstrated that the rest of

the preamble of claims 10 and 24 are disclosed by the Tailgate reference and that there are no genuine issues of material fact with respect to the preamble. (D.I. 421 at 14)

The first limitation of claims 10 and 24 is "receiving a packet comprising an ATA command block . . . comprising the ATA register accesses necessary to execute a given ATA register-delivered transaction." Toshiba's expert, Gardner, has demonstrated how Tailgate 4.3.1 "Register delivered command protocol" teaches this first limitation:

> For a register delivered command sent to the tailgate, the seven Command Block registers, excluding the Data register, will be used as the payload in the command block portion of the [Operation Request Block] ORB. Full details on the meaning and usage of these registers may be found in the ATA standard.

(D.I. 424, ex. 4 at 41) In other words, the host sends an IEEE 1394 packet to the tailgate bridge. The packet contains an ATA command block. "The tailgate shall write the seven Command Block register bytes to the device. The Device/Head register shall be the first written and the Command register shall be the last written by the tailgate. Order of transfer of all other registers is not defined." (*Id.*; *see also* D.I. 421 at 15-18; D.I. 422, ex. 4 at 4-8, 26-27)

The second limitation recites "parsing the command block into a sequence of ATA register operations." The court construed this limitation to mean "[r]etrieving a sequence of ATA register operations from the command block." (D.I. 277 at 19) Toshiba's expert, Gardner, has demonstrated that Tailgate teaches this limitation. Once the tailgate receives the command block, "[t]he tailgate performs all operations related to execution of ATA or ATAPI commands on the ATA bus. The tailgate determines what operations need to be performed based on information supplied in the ORB." (D.I. 424, ex. 4 at 36; *see also* D.I. 422, ex. 4 at 8-11, 27) Toshiba has demonstrated that there is no genuine issue of material fact with respect to this claim limitation. (D.I. 421 at 19-20)

The third limitation recites "communicating with an ATA device attached to the bridge via an ATA interface to execute the sequence of ATA register operations on the ATA device." The court construed "ATA interface" to mean "[c]omponent used to transmit ATA host signals to an ATA device and receive ATA device signals from the device." The parties agreed that an "ATA device" is "a data device that complies with an ANSI (American National Standards Institute) ATA standard." (D.I. 183 at 5) The Tailgate reference recites that "[t]he tailgate shall write the seven Command Block register bytes to the device. The Device/Head register shall be the first written and the Command register shall be the last written by the tailgate." (D.I. 424, ex. 4 at 41) "This executes the sequence of ATA register operations on the ATA device." (D.I. 421 at 20; *see also* D.I. 422, ex. 4 at 11-14, 27) There is no genuine issue of material fact with respect to this claim limitation. (D.I. 421 at 20-21)

The fourth limitation recites "when the given ATA register-delivered transaction requests the values for one or more registers on the ATA device, returning the register values to the host in packet format." The Tailgate reference specifies that

> [t]he tailgate's register delivered command request provides a mechanism to read the current contents of the Command Block registers without using a command to the connected device(s). When the tailgate receives such a command, it returns the current Command Block register contents without modifying the existing Command Block registers (other than the Device/Head register).

(D.I. 424, ex. 4 at 41) This is described in greater detail with reference to the bus interface unit and the initiator. (*Id.* at 28) The tailgate bridge reads the Command Block registers in the ATA device and returns the contents to the host. For example, within "initiator" operation, "[t]he tailgate processes the ORB, issues the command to the device, transfers data, reads Command Block registers at command completion, and returns their contents via the status block." (*Id.*) Also, for reads from the device, the Bus Interface Unit in the bridge "accepts the data that was read from the ATA bus," and

then "packages the data into one or more 1394 data packets, adds the appropriate information such as bus address and other control information, and transmits the packet to the initiator." (*Id.*) In other words, when an ATA transaction requests register values from an ATA device, the tailgate bridge obtains these register values from the ATA device and returns these values to the host computer in packet format. (*See also* D.I. 421 at 22) There is no genuine issue of material fact with respect to this claim limitation. (*Id.*)

The Tailgate reference only needs to disclose all the limitations of the claim with respect to one ATA register-delivered transaction in order to anticipate claims 10 and 24. *See Brown*, 265 F.3d at 1351 (Fed. Cir. 2001). Moreover, as discussed above, the "given ATA register-delivered transaction" limitations in these claims are "satisfied by at least one given ATA register-delivered transaction." (D.I. 486 at 33) Toshiba has met its burden and, through its expert, Gardner, has demonstrated that there are no genuine issues of material fact with respect to anticipation of these claims.[9] For these reasons, the court grants Toshiba's motion for partial summary judgment of invalidity of claims 10 and 24 of the '788 patent.

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[9] In response to Toshiba's anticipation argument, IV presented claim construction arguments. (D.I. 440 at 55-60) IV concluded its brief with the following:

> Toshiba and Mr. Gardner attempt to circumvent this defect [of the claim construction] by redrafting the claims so they are broad enough to encompass systems that can only execute a single command. That interpretation is incorrect for the reasons stated above—it is directly at odds with the stated purpose and advantages of the '788 patent described in the specification, it broadens the claims so much that they potentially cover the very ATAPI prior art distinguished in the patent, and it renders the claims nonsensical because they would include systems that, for all practical purposes, would be non-functional and useless. This incorrect interpretation advanced by Toshiba therefore should be disregarded, and Toshiba's motion should be denied.

(D.I. 440 at 60)

#### 4. Motion for relief

IV moves for relief with respect to invalidity of the '788 patent, because Toshiba allegedly failed to "analyze all the limitations of the asserted claims in [the] opening [expert] reports." (D.I. 460; D.I. 461 at 1) According to IV, in his opening report, Toshiba's expert did not "explain how the Tailgate reference allegedly meets the . . . [given ATA register-delivered transaction] limitations of the asserted . . . claims." (D.I. 460 at 7) Toshiba responds that its "experts provided thorough and complete invalidity expert reports on the . . . '788 patent[] that addressed each of the prior art references in question on a limitation-by-limitation basis."[10] (D.I. 481 at 9) As discussed above, the parties' invalidity dispute involved a question of claim construction raised for the first time in Dezmelyk's rebuttal expert report on validity. (D.I. 481 at 4) IV asserts that "Gardner subsequently analyzed these limitations for the first time in his supplemental expert report." (D.I. 461 at 7) Having reviewed the record in the case at bar, the court declines to grant relief.[11]

### B. '742 Patent

#### 1. Claim construction

In IV's infringement report, Dezmelyk presented a claim chart indicating that the accused products infringe claims 62 and 63 of the '742 patent; more specifically, the accused products practice the "data transfer speed" limitation by sending a descriptor called "bcdUSB," which indicates the USB specification release number associated with

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[10] (*See generally* D.I. 423; D.I. 424, ex. 4 (Exhibit D to Gardner's invalidity report))

[11] IV moves for relief with respect to noninfringement of the '788 patent because Toshiba's expert, Gardner, allegedly provided three new noninfringement theories in his rebuttal report. (D.I. 461 at 12) Toshiba argues that Gardner's rebuttal does not "constitute new defenses, but rather comprise additional details supporting existing defenses." (D.I. 481 at 18) The disputes documented by the parties are questions of fact relating to infringement, and the court has denied Toshiba's motion for noninfringement. Moreover, the court has found the '788 patent anticipated and denies this motion as moot.

the device. (D.I. 444, ex. 26, ex. A at 44) Toshiba responded that, on a claim construction in which a release number is a "data transfer speed," the ACCESS.bus 2.2 reference is invalidating prior art. (D.I. 492, ex. 1 at ¶ 52) IV moves for summary judgment of no invalidity of the '742 patent based upon Toshiba asserting an invalid "practicing the prior art" defense with respect to the ACCESS.bus 2.2 reference, an assertion Toshiba denies. (D.I. 486 at 11, 14) In the reply brief, IV again argues that Toshiba is asserting a "practicing the prior art" defense. (D.I. 538 at 6-7) Neither party has presented evidence or proposed language relevant to the construction of the "data transfer speed" limitation; therefore, the court lacks sufficient information to resolve this claim construction dispute on the record presented. The court declines to reach IV's motion for partial summary judgment of no invalidity with respect to the alleged "practicing the prior art" defense on this record.[12]

**2. Noninfringement**

Toshiba moves for partial summary judgment on the issue of whether the accused products infringe claims 57, 62, and 63 of the '742 patent. (D.I. 427; D.I. 434 at 32) The parties have stipulated that the accused USB products comply with the USB standards. (D.I. 494 at 31) Toshiba argues that USB-compliant products do not infringe the '742 patent, because the USB standard does not have a "bus interrupt line" as construed by the court. (D.I. 434 at 33-34) IV asserts that USB-compliant products infringe because, in the USB 2.0 or 3.0 specifications, a "practitioner would recognize . . . that the D+ line [is] being used as a 'bus interrupt line' at any time when data or protocol packets [are] not being actively transmitted on the bus."[13] (D.I. 442, ex. 1 at

[12] The court also declines to reach similar motions with respect to the '431 and '819 patents. (D.I. 426; D.I. 440 at 3)

[13] The "bus interrupt line" limitation is relevant to claim 57. Claims 62 and 63 involve a similar dispute over the "data transfer speed" limitation and whether or not these claims teach aspects of the USB standard. (D.I. 434 at 37-40; D.I. 494 at 36-40)

85) IV contends that "during those time intervals when a device attachment is possible, the line described in the Accused USB Standards is dedicated to detection of whether or not a device has been attached." (*Id.* at 85-86) Any discussion of limitations found in the USB standards that are not required by the claims at issue are irrelevant. The parties' arguments are all consistent with *Fujitsu*, 620 F.3d at 1327, i.e., if the parties have stipulated that the accused devices are USB compliant, then IV can prove infringement by comparing the claim limitations to the USB standard rather than to the elements of the accused devices. These issues of fact preclude summary judgment with respect to the '742 patent.

**3. No invalidity**

**a. ACCESS.bus reference**

IV moves for partial "summary judgment of no[] anticipation . . . because Toshiba and its experts agree that they lack at least one limitation of the relevant asserted claims. . . using claim constructions inconsistent with the court's order." (D.I. 426; D.I. 440 at 3) IV argues that "Toshiba's expert for the '742 patent, Robert Louis Stevenson ("Stevenson"), admits that the ACCESS.bus 2.2 does not anticipate the asserted claims of the '742 patent under the court's constructions."[14] (D.I. 440 at 4) Toshiba argues that Stevenson "offered this particular opinion based on IV's view of the Court's construction as reflected in IV's infringement theories." (D.I. 486 at 20) Toshiba asserts that "Dezmelyk[] contends that the peripheral sends the host a descriptor called 'bcdUSB,' which indicates the USB specification release number with which the peripheral complies. This release number does not itself indicate speed, but under IV's view of the court's construction, speed can be determined based on the release number." (*Id.* at 20-21) As discussed above, the court has insufficient information from

[14] Toshiba agrees. (D.I. 486 at 5)

the parties to resolve this question of claim construction and, therefore, denies IV's motion for summary judgment of no invalidity.

**b. USB 0.9 reference**

IV moves for summary judgment of no invalidity with respect to "USB 0.9, and the Motorola Envoy," because these references "are not even prior art." (D.I. 440 at 36) Toshiba has since withdrawn its defense with respect to the Motorola Envoy prior art.[15] (D.I. 486 at 2, n.1)

IV argues that there is no "evidence that [] inventions in USB 0.9 were actually conceived or that there was diligence in reducing USB 0.9 to practice during the period from August 18, 1995 until the alleged reduction to practice." (*Id.* at 36-37) Toshiba responds that the USB 0.9 specification is prior art under 35 U.S.C. § 102(g)(2), because it was conceived before August 18, 1995 and the inventors were reasonably diligent in reducing the USB 0.9 specification to practice in April 1996. (*Id.* at 25-28) In support, Toshiba presents evidence from a variety of sources documenting conception of USB 0.9 and reduction to practice over the following year. (*Id.*) IV disputes this evidence. (*See generally* D.I. 440 at 36-44) For example, IV disputes that USB 0.9 was conceived before August 18, 1995. (D.I. 440 at 39-40; D.I. 486 at 26) IV also argues that USB 0.9 could not have been reduced to practice, because it was replaced by USB 1.0. (D.I. 440 at 40; D.I. 486 at 26-27) Numerous factual disputes remain, and these are best addressed by a jury.

**C. '431 Patent**

**1. Claim construction**

The court construed "plurality of registers" as "two or more registers, each register exclusively associated with an array of memory cells." (D.I. 277 at 6) During

[15] The motion with respect to this reference, therefore, is denied as moot.

claim construction, the parties disputed whether the specification supported the idea of "transferring data through a single shared register." (*See, e.g.*, D.I. 231 at 12) The court addressed "whether two memory arrays may share the same register," and concluded "that each memory array is coupled to its own register." (D.I. 277 at 7) IV now argues that "the court's construction does not require that the 'exclusive association' [be] permanent." (D.I. 494 at 19) In support, IV presents argument and cites to an embodiment in the specification at col. 7, lines 5-18 in which "the registers are associated to different 'blocks of data' at different times using addresses." (D.I. 494 at 20) Toshiba responds that, under IV's proposed temporal exclusivity between registers and memory arrays, "there would be no difference between an 'exclusively associated' register and a 'nonexclusively associated' register." (D.I. 530)

Claim 1 recites a "plurality of arrays" and a "plurality of registers," but does not include the term "blocks." IV contends that the embodiment applies to the claims, because "at any given time, each register is exclusively associated with a particular block of memory based on those addresses. . . . [and a] block is itself an "array" because it is arranged in rows and columns." (*Id.* at 20-21) There is no indication that the applicant intended to include such a limitation in claim 1. Moreover, IV has not adequately explained how the '431 patent specification supports its assertion that "a block is itself an 'array.'"

"Exclusive" means "excluding or having the power to exclude (as by preventing entrance or debarring from possession, participation, or use)." *Merriam-Webster Unabridged* (2016). Under IV's proposal, exclusivity would not be "exclusive," because the register would not be able to exclude other memory arrays from associating with it. Moreover, Toshiba's expert, Vivek Subramanian ("Subramanian"), identified the relationship between the memory array, the "corresponding shift register 211," and the "data transfer circuitry" in the form of "internal bus 212" as central to the '431 patent.

('431 patent, abstract; figure 2, items 211, 212; 2:37, 3:24, 6:42-43, 6:49-50, 6:57, 7:1, 7:35, 7:43-44, 7:63, 8:42; 9:25) Subramanian explained that

> [o]ne of ordinary skill in the art would have understood that if the source array and destination array were associated with a common register [,i.e., the arrays were only temporally associated with the register], then data could be transferred from the source array to the destination array through the common register, bypassing the data transfer circuitry. However, . . . if the data could be transferred between the source and destination arrays without using the data transfer circuitry, then the data transfer circuitry would serve no purpose and the purported invention of the '431 patent would again be unnecessary.

(D.I. 202 at ¶ 21) "Data transfer circuitry" is a limitation of claim 1. Toshiba has provided unrebutted evidence that an architecture in which memory arrays share registers at different points in time would not need the "data transfer circuitry" as disclosed in the '431 patent and claimed in claim 1.

The court concludes that the claim language read in light of the specification suggests that each memory array is permanently coupled to its own register. *Fenner Investments, Ltd. v. Cellco P'ship*, 778 F.3d 1320, 1322-23 (Fed. Cir. 2015) ("The terms used in patent claims are not construed in the abstract, but in the context in which the term was presented and used by the patentee, as it would have been understood by a person of ordinary skill in the field of the invention on reading the patent documents."). Therefore, the court's claim construction reads: a "plurality of registers" is "two or more registers, each register exclusively, and permanently, associated with an array of memory cells." (D.I. 277 at 6)

**2. Motion for relief**

IV asserts that Toshiba did not originally present a source-code based noninfringement argument for the '431 patent until the rebuttal expert report on

noninfringement.[16] (D.I. 461 at 10) IV requests relief in the form of either a stricken rebuttal expert report or additional fact discovery to enable IV "to adequately respond to these new contentions." (*Id.* at 4) Toshiba responds that IV had adequate access to Toshiba's source code and that IV has not argued that its expert lacked adequate information to respond to questions during deposition by Toshiba's counsel. (D.I. 481 at 12-14) The record demonstrates that Toshiba did not provide IV with source-code based noninfringement contentions during fact discovery, and these contentions were first made available to IV in Toshiba's rebuttal expert report. The court grants IV's motion for additional fact discovery and orders Toshiba to make the company's 30(b)(6) witness(es) for the '431 patent available for one-day depositions, on the new non-infringement opinions, in New York City.

**3. Motion to strike**

Toshiba moves to strike McAlexander's supplemental expert report of infringement of the '431 patent, because this report "contain[s] opinions and evidence not timely disclosed." (D.I. 453 at 2; D.I. 454) IV responds that McAlexander was responding to new arguments presented by Subramanian in his rebuttal expert report. (D.I. 497 at 6) The court has ordered additional fact discovery from Toshiba's 30(b)(6) witnesses on the '431 patent and, rather than striking McAlexander's report, grants Toshiba additional fact discovery, in the form of a one-day deposition in New York City.

**4. Other pending motions**

Toshiba moves for partial summary judgment on the issue of whether the accused products infringe claims 1 and 2 of the '431 patent. (D.I. 427) IV moves for

[16] Indeed, IV contends that Toshiba's interrogatory responses on noninfringement of the '431 patent "did not include a single excerpt from any circuit schematic, source code, or circuit timing diagram." (D.I. 535 at 1)

partial summary judgment of no invalidity of the '431 patent. (D.I. 426) In light of the additional fact discovery with respect to the '431 patent, these motions are denied.

### D. '819 Patent

#### 1. Noninfringement

Toshiba moves for partial summary judgment on the issue of whether the accused products infringe claims 17 and 19 of the '819 patent. (D.I. 427; D.I. 434 at 13) Toshiba contends that "the accused Toshiba products do not . . . practice the 'writing the data' step of claim 17," because "the accused products do not transfer the same voltage level to the bitlines that was sensed on the bitlines in the prior 'sensing' step." (D.I. 434 at 13) For example, Toshiba's expert, R. Jacob Baker ("Baker"), explained that the "read value is inverted from the written value," which means that the voltage level is inverted and, therefore, is not the same. (D.I. 445, ex. 2 at ¶ 116) IV's expert, McAlexander, states in his supplemental report that this

> reasoning is flawed, because [Baker] focuses solely on the logical state at a certain node, which is labeled and referred to as SABL on the circuit schematic, . . . [but] Toshiba's datasheets make it clear that the data is not inverted during the read function, or during the read portion of the page copy or copyback function. . . . If a '1' is stored in page buffer, then a '1' will be transferred and stored in the memory cell. This '1' is represented by the amplified voltage level and will be transferred to the bitlines for writing data. The fact that the data, when it is read out of the memory cell, may be inverted (and then un-inverted) on its way to data cache has no bearing on whether the limitation "transferring said amplified voltage level to the bitlines for writing data" is met by the Accused Products.

(D.I. 443, ex. 3 at ¶ 69-71) These are disputes of fact that are best left to a jury. Therefore, the court denies Toshiba's partial motion for summary judgment of noninfringement of the '819 patent.

**2. No invalidity**

IV moves for partial summary judgment of no invalidity of the '819 patent in light of the TC5816 product. (D.I. 426; D.I. 440 at 5) According to IV's expert, McAlexander, "[t]he TC5816 Product does not anticipate claims 17 and 19 of the '819 patent . . . , because it [] writes an inverted version of the data to the source rows during a copy." (D.I. 440 at 27) Toshiba points out that McAlexander argued the opposite in his supplemental report:

> [W]hether the voltage level is inverted during some intermediate operation is not relevant to the claim, which simply requires "transferring said amplified voltage level to the bitlines for writing data," according to the court's construction. As long as the amplified voltage level is ultimately applied to the bitlines for writing data, the requirements of the claim and the court's construction are met.

(D.I. 443, ex. 3 at ¶ 66) "Accordingly, although Toshiba disagrees that inverted voltages can satisfy the court's claim construction . . . , Toshiba's expert," Robert J. Murphy ("Murphy"), "has applied that [] view of the court's constructions to the TC5816 prior art" for the purposes of invalidity. (D.I. 486 at 20) The court concludes that the parties' dispute does not rest on a question of claim construction;[17] instead, the experts disagree about whether the TC5816 product anticipates the claims, a question for the jury.

**3. IPR reference estoppel**

IV moves for summary judgment to prevent Toshiba from asserting invalidity challenges against the '819 patent, because Toshiba was the petitioner in an *inter partes* review ("IPR") in which the Patent Trial and Appeal Board ("PTAB") found several claims of the '819 patent invalid, including asserted claims 17 and 19. (D.I. 440 at 49; *see also* IPR2014-00418 (PTAB)) IV argues that "[o]ne of Toshiba's three elected

[17] Toshiba contends that this dispute is one of several involving claim construction issues. (D.I. 486 at 12)

grounds for invalidity—obviousness based on Ogawa '577 and Ogawa '045 and JP '832—was raised in the *inter partes* review of the '819 patent, and thus Toshiba is estopped from asserting invalidity on that ground in this action." (*Id.*) IV also argues that "[a]nother of Toshiba's three elected grounds for invalidity—obviousness based on Fuse '893 and Hiltebeitel '214 and knowledge of one of ordinary skill in the art—is based on publicly available patents and printed publications and could have been raised in the *inter partes* review of the '819 patent." (*Id.*) Toshiba responds that IV's request "is fundamentally unfair" and that "a stay – makes most sense, as the Federal Circuit appeal likely will result in the patent claims being confirmed as invalid." (D.I. 486 at 29)

Section 315(e)(2) of Title 35 of the United States Code provides in relevant part that "[t]he petitioner in an *inter partes* review of a claim in a patent under this chapter that results in a final written decision under section 318(a) . . . may not assert [] in a civil action arising in whole or in part under section 1338 of title 28 . . . that the claim is invalid on any ground that the petitioner raised or reasonably could have raised **during** that inter partes review." 35 U.S.C. § 315(e)(2) (emphasis added). Although IV's argument in this regard is perfectly plausible, in the sense that Toshiba certainly could have raised these additional obviousness grounds based on public documents at the outset of their IPR petition, the Federal Circuit has construed the above language quite literally. *See Shaw Indus. Grp., Inc. v. Automated Creel Sys., Inc.*, 817 F.3d 1293 (Fed. Cir. 2016) More specifically, the Court determined in *Shaw* that, because the PTAB rejected a certain invalidity ground proposed by the IPR petitioner, no IPR was instituted on that ground and, therefore, petitioner "did not raise – nor could it have reasonably raised – the [rejected] ground **during** the IPR." *Id.* at 1300 (emphasis in original) Although extending the above logic to prior art references that were never presented to the PTAB at all (despite their public nature) confounds the very purpose of this parallel

administrative proceeding, the court cannot divine a reasoned way around the Federal Circuit's interpretation in *Shaw*.

Toshiba may not raise obviousness based on Ogawa '577 and Ogawa '045 and JP '832 against the relevant claims of the '819 patent in the case at bar. However, Toshiba may present the additional invalidity grounds at trial.[18] For these reasons, the court grants-in-part and denies-in-part IV's motion.

**4. Motion for relief**

IV asserts that Toshiba did not originally present a source-code based noninfringement argument for the '819 patent until the rebuttal expert report on noninfringement.[19] (D.I. 461 at 10) IV requests relief in the form of either a stricken rebuttal expert report or additional fact discovery to enable IV "to adequately respond to these new contentions." (D.I. 461 at 4) Toshiba responds that IV had adequate access to Toshiba's source code and that IV has not argued that its expert lacked adequate information to respond to questions during deposition by Toshiba's counsel. (D.I. 481 at 12-14) IV argues that Toshiba's interrogatory responses on noninfringement of the '819 patent "did not include a single excerpt from any circuit schematic, source code, or circuit timing diagram." (D.I. 535 at 1) The record demonstrates that Toshiba did not provide IV with source-code based noninfringement contentions during fact discovery, and these contentions were first made available to IV in Toshiba's rebuttal expert report. The court grants IV's motion for additional fact discovery and orders Toshiba to make

[18] While the PTAB has ruled the relevant claims invalid, should the Federal Circuit overturn the PTAB, addressing these additional grounds at trial is more efficient than having to try invalidity on these grounds at a much later date. Therefore, Toshiba's request for a stay is denied.

[19] Indeed, IV contends that Toshiba's interrogatory responses on noninfringement of the '819 patent "did not include a single excerpt from any circuit schematic, source code, or circuit timing diagram." (D.I. 535 at 1)

the company's 30(b)(6) witness(es) for the '819 patent available for one-day depositions, on the new non-infringement opinions, in New York City.

### E. '270 Patent

#### 1. Claim construction

The parties disagree about the construction of the term "redundancy bus." (D.I. 434 at 7; D.I. 494 at 1) A "redundancy bus"[20] is an "address bus that allows for the addressing of the redundant memory cells independent of the addressing of the primary memory cells through the primary address bus." (D.I. 277 at 4) During claim construction, the court adopted Toshiba's proposal, but now the parties dispute whether the primary and redundancy buses must be separate wires or if a multiplexed bus, i.e., a single wire, may satisfy the claims.[21]

The specification differentiates the '270 patent from the prior art in which "[c]onventional RAM's (dynamic RAMs) [] disadvantageously employ a multiplexed addressing system." ('270 patent, 2:38-39) In the preferred embodiment, "both row and column address bits can be simultaneously presented to the address decoders 201. This feature eliminates the need for a multiplexed address bus." (*Id.*, 8:41-44) The preferred embodiment discloses a "non-multiplexed addressing scheme;" but "[a]lternatively, address bus 202 and redundancy address bus 301 may be multiplexed."

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[20] Found in claims 1, 3, and 20.

[21] Toshiba argues that "the [c]ourt's claim construction requires two address buses, a 'primary address bus' and a separate 'redundancy bus' that is independent from the primary address bus." (D.I. 434 at 7) IV argues that Toshiba is "using [a] claim construction[] inconsistent with the court's order." (D.I. 440 at 3) IV contends that "Toshiba's motion [] depends on reading in a limitation—that the 'redundancy bus' must be completely separate from the 'primary address bus,' and cannot have any overlap (e.g. shared lines). But the court's construction does not include the word 'separate' or any similar physical limitation." (D.I. 494 at 1)

(*Id.*, 10:26, 35, 52-53)) The specification explains how figure 4 operates in a multiplexed configuration:

> In this case, row address bits alone would be pipelined through row address amplifier/buffers 401 and redundancy address amplifiers/buffers 402 from address bus 202 and redundancy address bus 301 respectively. Similarly, in a multiplexed address system, only column address bits would be pipelined through column address amplifiers/buffers 406 and redundancy column address amplifiers/buffers 408. In the case of redundancy addressing, redundancy address bits to redundant rows are pipelined along with the remaining row address bits through buffer/amplifiers 402 and redundancy address bits to redundant columns are pipelined along with the remaining column address bits through buffers/amplifiers 408.

(*Id.*, 10:53-65) In the '270 patent, both the address system and the primary and redundancy buses may be multiplexed.

**2. Noninfringement**

Toshiba moves for partial summary judgment on the issue of whether the accused products infringe claims 1, 20, and 23 of the '270 patent. (D.I. 427; D.I 434 at 2) Toshiba contends that the products do not literally infringe the '270 patent, because they do not practice a "redundancy bus" under "the [c]ourt's claim construction [, which] requires two address buses, a 'primary address bus' and a separate 'redundancy bus' that is independent from the primary address bus." (D.I. 434 at 7) Toshiba argues that IV's allegations of a multiplexed bus under the doctrine of equivalents is barred by the disclosure dedication doctrine.

IV's expert, McAlexander, presented facts to demonstrate that the accused NAND flash products use separate address spaces for primary cells and redundant cells. For example, in the relevant Toshiba source code, "the title identifies the Local and Remote RD sets which relate to the 'LRDSEL' and 'RRDSEL' signals respectively. The Local set is the primary cells and the remote are the redundant cells." (D.I. 443, ex. 1 at ¶ 166) IV presented additional facts to demonstrate infringement. (*See, e.g.*, D.I.

494 at 7-8) Meanwhile, Toshiba continues to argue its alternate claim construction and has cited to numerous disagreements with IV's experts. (D.I. 434 at 7-13) The court's claim construction supports a multiplexed bus; therefore, Toshiba's motion is denied. IV's doctrine of equivalents argument is not barred by the disclosure dedication doctrine, because numerous facts remain in dispute.

**3. Claim priority**

Toshiba moves that claims 1, 20, and 23 of the '270 patent all include the term "redundancy bus," which is new matter and, therefore, is not entitled to the priority date of the '822 or '573 patents. (D.I. 420; D.I. 421 at 5-6) IV responds that a person of ordinary skill in the art would understand that the '573 and '822 patent specifications support addressing of redundant memory cells independent of the primary memory cells. (D.I. 440 at 55)

The '270 patent (filed Feb. 1, 1996) is a continuation-in-part of U.S. Pat. No. 5,583,822 (the '822 patent, filed Nov. 1, 1995), which is a continuation of U.S. Pat. No. 5,473,573 (the '573 patent, filed May 9, 1994). The '573 patent discusses redundant memory cells:

> Each memory block includes n number of data lines 203 coupled to controller 103 via an m-bit wide data bus 204. Further, each memory block includes a number of redundant cells 205 (along with peripheral circuits such as sense amplifiers and enable/disable fuses) for repairing defective cells by substitution.

('573 patent, 6:34-39) Redundant memory cells are included in memory blocks alongside primary memory cells. The specification also discusses addressing:

> In the illustrated embodiment, four memory blocks 200a-200d are provided each of which contains an array of memory cells arranged as X number of rows and Y number of columns and configured, output a n-bit words per address. Each memory block is associated with an address decoder 201. Addresses of j number of bits are provided to each decoder 201 from controller 103 via a j-bit wide address bus 202. Preferably, each decoder 201/block 200 responds to a different range of addresses in the

> controller address space. . . . Further, each memory block includes a number of redundant cells.

('573 patent, 6:26-37) IV asserts that a decoder associated with a memory block responding to a range of addresses is the same as the "independent addressing" aspect of the court's claim construction, and that by disclosing "independent addressing," the '573 patent disclosed the "redundancy bus," thereby giving claims 1, 20 and 23 of the '270 patent the priority date of the '573 patent. (D.I. 440 at 54)

The court construed "redundancy bus" to be an "address bus that allows for the addressing of the redundant memory cells independent of the addressing of the primary memory cells through the primary address bus." (D.I. 277 at 4) The '573 patent discloses an "address bus" as well as primary and redundant memory cells, but the '573 patent does not disclose a redundancy (address) bus.[22] Moreover, the '573 patent does not disclose independent addressing of the primary and redundant memory cells. For example, even if, as IV argues, the range of addresses associated with a given decoder/memory block combination is an independent address space, the redundant memory cells are not addressed "independent of the addressing of the primary memory cells,"[23] because the primary and redundant memory cells are located within the same memory block and, therefore, are within the same independent address space.

The '573 patent does not disclose an "address bus that allows for the addressing of the redundant memory cells independent of the addressing of the primary memory cells through the primary address bus;"[24] therefore, the '573 patent does not disclose the "redundancy bus" found in the '270 patent. For this reason, the "redundancy bus" of the '270 patent constitutes new matter, and claims 1, 20, and 23 of the '270 patent are

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[22] The court noted in its construction that the specification (with reference to figure 2) also does not discuss a redundancy bus. (D.I. 277 at 4)

[23] (*See* D.I. 277 at 4)

[24] (*See* D.I. 277 at 4)

not entitled to the priority date of the '573 patent.[25] Toshiba's motion is granted. The priority date of claims 1, 20, and 23 of the '270 patent is the filing date of the '270 patent, which is February 1, 1996.

**4. No invalidity**

IV moves for summary judgment of no invalidity of the '270 patent in light of the McClure and Sukegawa references, as well as the TC5816 product. (D.I. 426; D.I. 440 at 3) IV's expert, McAlexander, argues that "the redundancy bus is not required to be separate from the primary address bus . . . [and] the '270 patent specifically teaches that information on both primary and redundancy busses may be multiplexed." (D.I. 443, ex. 2 at 50) Toshiba's expert, Subramanian, disagrees, because "McAlexander provides no explanation or analysis of how the single address bus structure he identifies . . . meets the court's construction of redundancy bus."[26] (D.I. 448, ex. 2 at ¶ 30) IV argues that Subramanian relies on an "oversimplified definition" that misses McAlexander's analysis that "the primary address bus and redundancy bus can have some overlap, but also have some lines that are dedicated to redundancy information." (D.I. 440 at 22) At this stage, the parties disagree whether, for purposes of anticipation, a "single multiplexed bus" is the same as two buses with "some overlap." (D.I. 440 at 22; D.I. 443, ex. 1 at A-a13, A-a15) This is a factual question for the jury.

**5. Motion for relief**

IV moves for relief with respect to invalidity of the '270 patent, because Toshiba allegedly failed to "analyze all the limitations of the asserted claims in [the] opening [expert] reports." (D.I. 460; D.I. 461 at 1) Not surprisingly, this motion practice devolved into a finger-pointing exercise about the alleged failures of the respective experts. The

[25] For similar reasons, the claims are not entitled to the priority date of the '822 patent.
[26] This disagreement centers on the construction of "redundancy bus" addressed above.

court declines to address this motion on this record, but will note objections at trial based on such deficiencies.

**F. Damages**

IV moves for summary judgment of no available, acceptable non-infringing alternatives of the '788, '742, '431, '819, and '270 patents. (D.I. 426) Toshiba moves to exclude opinions and testimony of Teece, IV's damages expert. (D.I.449) IV moves to exclude testimony of Davis, Toshiba's damages expert. (D.I. 457) Given the complexity of the litigation at bar, in the interest of judicial efficiency, the court will to bifurcate damages. *See Robert Bosch, LLC v. Pylon Mfg. Corp.*, 719 F.3d 1305, 1319 (Fed. Cir. 2013) ("district courts, in their discretion, may bifurcate willfulness and damages issues from liability issues in any given case."). These motions, therefore, are denied without prejudice.

## V. CONCLUSION

For the foregoing reasons, the court grants Toshiba's motion for partial summary judgment of claim priority as to U.S. Patent No. 5,701,270 and for summary judgment of invalidity as to U.S. Patent No. 6,618,788 (D.I. 420), denies without prejudice IV's motion of no available non-infringing alternatives to U.S. Patent No. 6,618,788, U.S. Patent No. 5,938,742, U.S. Patent No. 5,568,431, U.S. Patent No. 5,500,819, and U.S. Patent No. 5,701,270 (D.I. 426), denies IV's motion for partial summary judgment of no invalidity of U.S. Patent No. 6,618,788, U.S. Patent No. 5,938,742, U.S. Patent No. 5,568,431, U.S. Patent No. 5,500,819, and U.S. Patent No. 5,701,270 (D.I. 426), grants in part and denies in part IV's motion for partial summary judgment of statutory estoppel of U.S. Patent No. 5,500,819 (D.I. 426), denies Toshiba's motion for summary judgment of noninfringement of U.S. Patent No. 6,618,788, U.S. Patent No. 5,938,742, U.S. Patent No. 5,568,431, U.S. Patent No. 5,500,819, and U.S. Patent No. 5,701,270 (D.I.

427), denies without prejudice Toshiba's motion to exclude David J. Teece's opinions and testimony (D.I. 449), denies Toshiba's motion to strike Joseph McAlexander's supplemental expert report (D.I. 453), denies without prejudice IV's motion to exclude testimony of Julie L. Davis (D.I. 457), grants in part and denies in part IV's motion for relief (D.I. 460), and denies Toshiba's request for a stay of proceedings with respect to U.S. Patent No. 5,500,819 (D.I. 486).

An appropriate order shall issue.